ABSTRACT OF THE DISCLOSURE

An insulating device for system on chip (SOC). The SOC has a first circuit region powered by a main power source and a second circuit region powered by a real-time power source. In the insulating device, a selector designates the main power source or a battery source as a real-time power source. A level detector detects a voltage level of the main power source and outputs a resulting signal. A NAND gate produces a logic output according to the result signal and an output signal of the first circuit. The NAND gate includes first and second PMOS transistors and first and second NMOS transistors. Gates of the first PMOS transistor and the first NMOS transistor are directly connected to the output signal of the first circuit without through any buffers. Gates of the second PMOS transistor and the second NMOS transistor are directly connected to the result signal without any buffers.